

**1-day WORKSHOP ON
VARIABILITY AND RELIABILITY RESEARCH IN DEVICES, CIRCUITS AND SYSTEM IN
ADVANCED TECHNOLOGIES
ESSCIRC conference (<http://esscirc2013.imt.ro/>)
September 20th 2013**

Organizers: Asen Asenov and Antonio Rubio

**Under the framework the FP7 European Projects TRAMS, MORDRED and
SUPERTHEME**

Preliminary organization:

8.50 Welcome and introduction, Asen Asenov(1), Antonio Rubio(2)

9.00 Keynote on project SupertHEME(A): "Circuit Stability Under Process Variability and Electro-Thermal-Mechanical Coupling", Juergen Lorenz(3) (20'+10')

9.30 Keynote on project Mordred(B): "Modelling of the reliability and degradation of next generation nanoelectronic devices", Tibor Grasser(4) (20'+10')

10.00 Keynote on project TRAMS(C): "Terascale Reliable Adaptive Memory System", Antonio Rubio, UPC, (20'+10')

10.30 Coffee break

11.00 Talk(D): "A Multi-scale Approach from First Principles to TCAD Time-Dependent Variability Simulations", Alexandre Shluger(5), University College of London, Tohoku University (25'+5')

11.30 Talk(E): "Interplay between statistical variability and reliability and impact on design", Asen Asenov, UOG, (25'+5')

12.00 Lunch

13.30 Talk (G): "Modelling process and statistical variability in devices and circuits." C. Millar(7), GSS (25'+5')

14.00 Talk(H): "Characterization of BTI induced variability in scaled Metal Gate / High-K CMOS technologies", Andreas Kerber(8), Global Foundries (25'+5')

14.30 Talk(I): "Time-dependent variability in advanced CMOS technologies: from nanoscale mechanisms to circuit level assessment", Montserrat Nafria(9), UAB, (25'+5')

15.00 Coffee Break

15.30 Talk(F): "FinFETs and their impact on SRAM and DRAM memories", Ramon Canal(6), UPC, (25'+5')

16.00 Talk(J): "Tool procedures to evaluate reliability under variability effects", Elena Ioana Vatajelu(10), LIRMM

16.30 Talk (K): “Modeling of Local Layout Effects and Statistical Variability for Circuit Design”, A. Juge(11), ST Microelectronics

17.00 Closing of the workshop

BIOGRAPHY OF SPEAKERS:

(1) Prof. Asen Asenov, University of Glasgow, UOG

Asen Asenov (FIEEE, FRSE) is a founder and CEO of Gold Standard Simulations (GSS) Ltd. (www.goldstandardsimulations.com). GSS is the leader in physical simulation of statistical variability, statistical compact model extraction and generation technology and statistical circuit simulation. As a James Watt Professor in Electrical Engineering at Glasgow University and Leader of the 30 members strong Glasgow Device Modelling Group (<http://web.eng.gla.ac.uk/groups/devmod/>)

(2) Prof. Antonio Rubio, Polytechnical University of Catalonia, UPC

Antonio Rubio is professor of the Electronic Engineering Department at UPC, Barcelona Spain.

(3) Dr. Juergen Lorenz, Fraunhofer Institute, IISB

Juergen K. Lorenz was born in Stockelsdorf, Germany, in 1957. He obtained his degrees in mathematics and physics (“Diplom-Mathematiker” and “Diplom-Physiker”) from the Technical University of Munich in 1982 and 1984, respectively, and the PhD in electrical engineering (Dr.-Ing.) from the University of Erlangen-Nuremberg in 2000.

He joined Fraunhofer in 1983. Since 1985 he is in charge of the technology simulation department of the then newly founded Fraunhofer IISB in Erlangen. His main subjects are the development of physical models and programs for semiconductor process simulation and the required algorithms. He authored or co-authored about 120 papers, and has repeatedly been or is member of the technical committees of the ESSDERC, SISPAD, and IEDM conferences. During the last 18 years he has been involved in 30 European projects, for 8 of which he acted as coordinator.

Dr. Lorenz is member of IEEE and the ECS. Following requests from industry he contributes since 2000 as expert to the preparation of the International Technology Roadmap on Semiconductors, and is chairman for its Modeling and Simulation chapter since 2002.

(4) Prof. Tibor Grasser, TU Wien

Tibor Grasser received his Ph.D. degree in technical sciences from TU Wien where he is currently employed as an Associate Professor. In 2003 he was appointed director of the Christian Doppler Laboratory for TCAD in Microelectronics. Dr. Grasser is the co-author or author of more than 400 scientific articles, editor of a book on advanced device simulation, a distinguished lecturer of the IEEE Electron Devices Society, a senior member of IEEE, has been involved in various functions of outstanding conferences such as IEDM, IRPS, SISPAD, IWCE, ESSDERC, IIRW, and ISDRS, is a recipient of the Best Paper Awards at IRPS (2008, 2010, and 2012), ESREF (2008) and the IEEE EDS Paul Rappaport Award (2011). He was also a chairman of SISPAD 2007 and is currently TPC chair of IIRW 2013.

(5) Prof. A. L. Shluger, University College London

Alexander Shluger graduated from the Latvia State University, Riga, USSR in 1976, received Ph.D and Doctor of Science degrees from the L. Karpov Physics and Chemistry Research Institute, Moscow in 1981 and 1988, respectively. He joined the Royal Institution of Great Britain, London in 1991 and the faculty of the University College London in 1996, where he is a Professor of Physics from 2004. He has been appointed a head of Condensed Matter and Materials Physics group in 2006. He is a Fellow of the Institute of Physics and of the American Physical Society, a Foreign Member of the Latvian Academy of Sciences and a Principal Investigator at the WPI-Advanced Institute of Materials Research, Tohoku University, Japan. Main research interests concern the mechanisms of defect related processes in the bulk and at surfaces of insulators. Current research is focused on theoretical studies of defects in oxides in relation to reliability of CMOS devices, the mechanisms of photo-induced processes at oxide surfaces, and on modelling of imaging and manipulation of molecular specie at insulating surfaces using Atomic Force Microscopy.

(6) Dr. Ramon Canal, UPC

Ramon Canal received the MS and PhD degrees from the Universitat Politècnica de Catalunya (UPC). He joined the faculty of the Computer Architecture Department of UPC in 2003. He worked at Sun Microsystems in 2000, and he was a Fulbright visiting scholar at Harvard University in 2006/2007. His research focuses on power and thermal aware circuits and architectures, as well as reliability and memory hierarchy. He has an extensive list of publications and several invited talks both in industry and academia.

(7) Dr. C. Millar, GSS

Campbell Millar (M09) received his PhD in 2003 from the University of Glasgow. He is currently the Chief Operations Officer and Head of Software Development at Gold Standard Simulations Limited, based in the UK. Before moving to GSS he was a Senior Research Fellow in the School Engineering of the University of Glasgow.

(8) Dr. Andreas Kerber, GLOBALFOUNDRIES

Andreas Kerber was born in Schnann, Austria, and received his Diploma in physics from the University of Innsbruck, Austria, in 2001, during which time he was working at Bell Laboratories, Lucent Technologies (Murray Hill, NJ, USA) on the electrical characterization of ultra-thin gate oxides. In 2001, he joined Infineon Technologies in Munich, Germany. From 2001 to 2003, he was assigned to International SEMATECH at IMEC in Leuven, Belgium, where he was involved in the electrical characterization of alternative gate dielectrics for sub-100 nm CMOS technologies. At the same time he fulfilled the requirements for a PhD in electrical engineering and defended his thesis at the TU-Darmstadt, Germany, with honors. From 2004 to 2006, he was with the Reliability Methodology Department at Infineon Technologies in Munich, Germany, responsible for the dielectric reliability qualification of process technology transfers of 110 and 90 nm memory products. At the same time he developed a fast wafer-level data acquisition setup for time-dependent dielectric breakdown (TDDB) testing with sub-ms time resolution. In 2006, he joined AMD and now is with GLOBALFOUNDRIES in Yorktown Heights, NY, working as a Senior Member of Technical Staff on front-end-of-line (FEOL) reliability research with focus on metal gate / high-k CMOS process technology, advanced transistor architecture and device-to-circuit reliability correlation. Dr. Kerber has contributed to more than 80 journal and conference publications and presented his work at international conferences, including the VLSI Technology Symposium, the International Electron Device Meeting (IEDM) and the International Reliability Physics Symposium (IRPS). In addition, he has presented invited talks at the

Workshop of Dielectrics in Microelectronics (WoDIM), the Semiconductor Interface Specialist Conference (SISC) and given tutorials on metal gate / high-k reliability characterization at the International Integrated Reliability Workshop (IIRW) and IRPS. Dr. Kerber has served as a technical program committee member for the SISC (2006, 2007), IRPS (2007, 2011, 2012), IEDM (2011, 2012) and Infos (2013).

(9) Prof. Montserrat Nafria, UAB

Montserrat Nafria received the Ph.D. degree in Physics from the Universitat Autònoma de Barcelona, Spain, in 1993, where she is currently a Full Professor at the Department of Electronic Engineering. Her major research interests include CMOS device and circuit reliability. Currently, she is working on the characterization and modelling of the aging (BTI and channel hot carrier degradations) and variability of advanced MOS devices. This is done from the nanoscale level, by studying the phenomena using Atomic Force Microscope-related techniques, up to circuit level, by developing device models for circuit simulators that account for their time-dependent variability. She is also interested in the characterization and modelling of Resistive-Switching devices. She is the author or coauthor of more than 200 research papers in scientific journals and conferences in all these fields.

(10) Dr. Elena Ioana Vatajelu, LIRMM

Ioana Vatajelu received the MS degrees in Physics from the Babes-Bolyai University in Cluj Napoca in 2004 and in Control Engineering from the Technical University of Cluj Napoca, Romania in 2006. She received her PhD degree in Electronic Engineering in September 2011 from the Universitat Politècnica de Catalunya (UPC), Spain. She is currently post-doctoral researcher at LIRMM Laboratory in Montpellier, France. Currently, her research is focused on variability aware memory design and test.

(11) Dr. Jugé, ST Microelectronics R&D

André Juge graduated with a PhD degree from Université Scientifique et Médicale de Grenoble. Starting 1988, he held positions as Modeling Engineer and Team leader in STMicroelectronics R&D, to support development of BICMOS and CMOS technologies. In 2002, he became Modeling manager within Crolles2 Alliance, France, to support the development of 90nm, 65nm, and 45nm Bulk CMOS technologies. Since 2007, his activities are devoted to Advanced modeling solutions through cooperative projects with Academia, Compact Model Council (CMC), and EDA tool suppliers.

SUMMARY OF TALKS

(A) SUPERTHEME project: <http://www.supertHEME.eu/>

Among the physical limitations which challenge progress in nanoelectronics for aggressively scaled More Moore, Beyond CMOS and advanced More-than-Moore applications, process variability and the interactions between and with electrical, thermal and mechanical effects are getting more and more critical. Effects from various sources of process variations, both systematic and stochastic, influence each other and lead to variations of the electrical, thermal and mechanical behavior of devices, interconnects and circuits. Correlations are of key importance because they drastically affect the percentage of products which meet the specifications. Whereas the comprehensive experimental investigation of these effects is largely impossible, modelling and simulation (TCAD) offers the unique possibility to predefine process variations and trace their effects on subsequent process steps and on devices and circuits fabricated, just by changing the corresponding input data. This important requirement for and capability of simulation is among others highlighted in the International Technology Roadmap for Semiconductors ITRS. A project partner has also demonstrated how correlations can be simulated.

Within SUPERTHEME, the most important weaknesses which limit the use of current TCAD software to study the influence of both systematic and stochastic process variability and its interaction with electro-thermal-mechanical effects will be removed, and the study of correlations will be enabled. The project will efficiently combine the use of commercially available software and leading-edge background results of the consortium with the implementation of the key missing elements and links. It will bridge the current critical gap between variability simulation on process and device/interconnect level, and include the treatment of correlations. The capabilities of the software system will be demonstrated both on advanced analog circuits and on aggressively scaled transistors.

(B) MORDRED project: Modelling of the reliability and degradation of next generation nanoelectronic devices <http://webhotel2.tut.fi/fys/mordred/>

The aim of the MORDRED project is to develop multiscale modelling technology, supported by comprehensive experimental characterization techniques, to study the degradation and reliability of next generation CMOS devices. Building upon fundamental analysis of the structure and electronic properties of relevant materials and interfaces at the quantum mechanical level, mesoscale models are under construction to account for defect generation and their impact on transistor and CMOS circuit performance and yield. Upon completion, the project will provide technologists, device engineers and designers in the nano CMOS industry with tools, reference databases and examples of how to produce future generation devices that are economical, efficient, and meet high performance, reliability and degradation standards.

(C) TRAMS project: Terascale Reliable Adaptive Memory Systems <http://www.trams-project.eu/>

Technology projections indicate that future electronic devices will keep shrinking, being faster and consuming less energy per operation. In the next decade, a single chip will be able to perform trillions of operations per second and provide trillions of bytes per second in off-chip bandwidth. This is the so called Terascale Computing era, where terascale performance will be mainstream, available in personal computer, and being the building block of large data centers with petascale computing capabilities. However, these smaller devices will be much more susceptible to faults and its performance will exhibit a significant degree of

variability. As a consequence, to unleash these impressive computing capabilities, a major hurdle in terms of reliability has to be overcome. The TRAMS project is the bridge for reliable, energy efficient and cost effective computing in the era of nanoscale challenges and teraflop opportunities.

Talk (D): A Multi-scale Approach from First Principles to TCAD Time-Dependent Variability Simulations

Oxide aging and particularly Negative Bias Temperature Instability (NBTI) is one of the major threats for device reliability. All traps related effects are now considered as a time-dependent variability, drastically impacting design margins. A robust design aiming at oxide reliability impacts reduction relies on a better understanding of the traps properties and, in turn, of their dynamics and their impact on devices, including their interaction with the statistical variability (SV) induced by the atomistic nature of dopants. In this work we present for the first time a unified simulation framework from the first principles simulations to TCAD statistical simulations of the time-dependent impact of NBTI on device performances. We review some of the theoretical models proposed for oxygen deficient defects in silica and hafnia and their charge trapping behaviour. Defect properties obtained by first principles simulations of Si/SiO₂ interfaces are used as an input in a drift diffusion simulator, including a physics-based trapping/detrapping model in presence of SV. Existing compact model extraction tools can easily extend these results to the ultimate multiscale simulation tool, from first principles to circuit simulations.

Talk (E): Interplay between statistical variability and reliability and impact on design

Statistical variability arising from the discreteness of charge and granularity of matter is a critical concern in device scaling. Simultaneously interface/oxide trapping/detrapping events could result in degradation and time dependent evolution of the statistical variability. The impact of individual and multiple charge trapping events depends of the underlying sources of statistical variability. The interplay between the statistical variability and reliability depends of the device architecture and design and is different in bulk, FDSOI transistors and FinFETs. Simultaneously the time dependent, BTI and NCI related variability affect adversely the lifetime of variability sensitive circuits like SRAM. In this talk we will highlight the differences in the interplay between statistical variability and reliability in contemporary and future CMOS technologies and its impact on circuit and system design.

Talk (F): FinFETs and their impact on SRAM and DRAM memories

FinFET technology brings the promise of reduced variability and leakage currents. In this talk, I will first present the evolution of memory cell technology and sizes in the recent years. Then, I will analyze the consequences of building memory cells with FinFETs. I will quantify the benefits in both SRAM and DRAM cell types.

Talk (G): "Modelling process and statistical variability in devices and circuits."

TCAD modelling and simulation provides a powerful tool for the study of the impact of statistical and process variability on the performance of modern CMOS devices. The interactions between local statistical variability from random sources such as Random Discrete Dopants, Line Edge Roughness and gate material granularity, and more deterministic device variability typically introduced by process variations are complex and require advanced device simulation, compact model extraction and circuit simulation techniques. In order to ensure product functionality and yield with advanced technologies it is necessary accurately model the impact of device level variability on circuits and systems such as SRAM. In this talk we will consider the advanced TCAD and compact modelling

techniques which are required to accurately capture the impact of variability on the performance of circuits and systems.

Talk (H): Characterization of BTI induced variability in scaled Metal Gate / High-K CMOS technologies

Time-zero and time dependent variability is a growing concern for aggressively scaled transistor technologies with metal gate/high-k stacks. Bias temperature instability (BTI) in PMOS as well as NMOS devices is considered the most dominant time dependent variability component and needs to be modeled using stochastic processes. The physical nature of the stochastic process is still under debate and to support the model development efforts large statistical data sets are essential. In this presentation, we will focus on the characterization challenges related to stochastic BTI process in small area CMOS devices and discuss the large scale data we collected on discrete SRAM and logic devices. Finally we will elaborate on the impact of BTI induced variability on End-of-Life threshold voltage distributions and show that BTI induced variability is not the major contributing factor in the post stress threshold voltage variability in planar metal gate/high-k CMOS devices.

Talk (I): Time-dependent variability in advanced CMOS technologies: from nanoscale mechanisms to circuit level assessment

In ultra-scaled devices, because of the aging mechanisms that can be triggered during the device operation, the process-related variability turns into a time-dependent variability, so that the device electrical behavior must be described by statistically distributed parameters that evolve with time. Device aging depends on its particular operation in the IC (i.e., circuit topology, voltages, frequency, duty cycle, temperature...), so that it must be evaluated in a circuit context. Moreover, device time-dependent variability translates into shifts of the circuit parameters, leading to a loss of circuit performance and/or reliability. To establish the link between device aging and circuit operation/performance, statistical circuit simulation, which considers device aging (and also the initial variability), will be needed to capture the time-dependent device/circuit parameter variations. Therefore, a combination of Monte Carlo (to account for variability) and SPICE simulations (to consider the particular circuit configuration and device stress conditions) seems the most suitable approach. In this simulation methodology, the description of the device time-dependent variability is actually the clue for accurate simulations. Therefore, physics-based models of the aging phenomena, whose parameters account for the underlying fabrication technology and operation dependences, are required.

This work is focussed on the most important aging mechanisms in MOSFETs, i.e., Bias Temperature Instabilities (BTI), Channel Hot Carrier (CHC) degradation and Time Dependent Dielectric Breakdown (TDDB), using a multilevel approach, starting at the nanoscale and ending at circuit level. The atomic-scale origin of the different aging mechanisms will be discussed and their most important effects on the device electrical behaviour described, together with examples of physical models for the aging. Emphasis will be done on the electrical characterization of device aging for model parameter extraction. How the effects of process variability, BTI aging and TDDB effects at device level can be considered (with the aid of the physical models) during circuit simulation will be shown, by describing the main features of RELAB, an example of statistical circuit simulation tool. Some circuit simulation examples will show that such kind of tool can be used to identify the weakest devices in a circuit and to evaluate the circuit performance degradation, so that it could be used by circuit

designers for circuit performance and reliability improvement, early during the design phase of the circuit.

Talk (J): Statistical Robustness Analysis of Nanometric SRAM Memories under Process Variability

The memory structures are critical to any large, complex digital design. There are two main concerns with regard to the reliability of nanometric memories in general and to Static Random Access Memories (SRAM) in particular: technology scaling and supply voltage scaling. With the continuous technology scaling, the robustness of the SRAM memories becomes an important concern for the design and test engineers. Maintaining an acceptable level of robustness in SRAMs while scaling the minimum feature size and supply voltages of Systems-on-a-Chip (SoC) becomes increasingly challenging. Pushing the physical limits of scaling leads to device patterning challenges and non-uniform channel doping. In order to improve system performance, large arrays of fast SRAM are required, but the area impact of incorporating large SRAM into a chip translates into a higher chip cost. As a result, minimum-size SRAM cells are tightly packed, making SRAM arrays the densest circuitry on a chip. This is the reason why the SRAM arrays are the most susceptible and sensible to manufacturing defects and process variations. Any asymmetry in the SRAM cell structure will make the cell less robust. The expected difficulties with scaling the SRAM are maintaining both acceptable noise margins (static and dynamic) and controlling its functionality. This presentation is focused on analyzing the SRAM cell's robustness and functionality under process and environmental variations and providing new and easy to use metrics for robustness and functionality evaluation of the SRAM cell for parametric yield estimation.

Talk (K): Modeling of Local Layout Effects and Statistical Variability for Circuit Design

Circuit design techniques for First-Silicon success in modern CMOS technologies require accurate and efficient simulation methodologies to handle both Process and Layout variations. The presentation is focused on Local variability at transistor scale, including Systematic Variability induced by local layout effects and Statistical Variability induced by local random fluctuations. In the process to define solutions applicable for Circuit Design in Industry, we consider accuracy/efficiency requirement per Circuit block, and important implementation aspect in the area of device characterization, compact modeling, and circuit simulation flow. The presentation will be illustrated by examples representative of Modern CMOS technologies.