CASTNESS 2013

June 28th, Campus Nord UPC, Aula Master

PRELIMINARY AGENDA

9.00 Welcome and introduction
9.10 90 MINUTES SLOT FOR TRAMS PROJECT

- ✓ "Overview of the TRAMS project", Antonio Rubio
- ✓ "Controlled Degradation Stochastic Resonance in Future Nanoarchitectures", Nivard Aymerich
- ✓ "New cells and reliability mechanisms for next generation memories", Ramon Canal
- ✓ "PERFORMANCE, POWER AND RELIABILITY AWARE DESIGNS FOR TERA-SCALE PROCESSORS" , Tanatsu Ramírez, Intel
- ✓ "Dynamically Capturing Vulnerability Variation for Caches", Javier Carretero, Intel

10.40 Coffee break

11.20 100 MINUTES SLOT FOR EURETILE PROJECT

- ✓ "Distributed application layer: mapping dynamic applications on many-core systems", Iuliana Bacivarov, ETH Zurich
- ✓ "Full Methodology of a Lightweight Task Migration in Embedded Multi-Tiled Architecture Using Task Code Replication", Ashraf ELANTABLY, TIMA
- ✓ "The EURETILE parallel simulation environment", Jan H. Weinstock, RWTH Aachen
- ✓ "The EURETILE hardware experimental platform" - Andrea Biagioni, INFN-TARGET
- ✓ "Fault and critical event awareness: a no single point of failure approach for distributed systems" - Laura Tosoratto, INFN-TARGET

13.00 Lunch time

14.15 60 MINUTES SLOT FOR SOOS PROJECT

- ✓ "Overview over SoOS and the main results", Lutz Shubert
- ✓ "CλaSH - A Functional Hardware Description Language", Christiaan Baaij, University of Twente

15.15 90 MINUTES SLOT FOR TERAFLUX

- ✓ "The T* Instruction Set Extension", Roberto Girogi, UNISI

- ✓ "Analysis and RTL Simulation of the Task Superscalar Architecture Hardware", Carlos Alvarez, UPC
- ✓ "From Scala to C++. Integrating Scala based dataflow programs into the TERAFLUX tool chain", Daniel Goodman, UNIMAN

16.45 CONCLUSIONS and CLOSING
17.15 --