TRAMS PROJECT

FP7 248789

Proposal of changes in the DoW

March 15th 2010

1. INTRODUCTION

After the Kickoff meeting held last February 1st, in Barcelona, following the conclusions of the meeting, the respective leaders of each Work package together with the corresponding participants and with the supervision by the Coordinator as well as the Project Management Board, have reviewed in detail the objectives, the input/output of each task, the milestone and deliverables description and coordination and timing.
From this action a small number of null or low impact changes are proposed, requiring the permission of the EC in order to be considered.

2. LEVEL OF THE CHANGES

The changes proposed do not modify at all the objectives, or the PM assignment per institution, the list of deliverables and main description of each one. The changes affect only the order of few deliverables. Finally there is a small movement of 4.5PMs from WP2 to WP4 affecting the IMEC participation.

3. CHANGES IN WORK PACKAGE 1

Due to a more reasonable sequence of work delivery the required change is:

- **Exchange of deliverables D1.2 and D1.3,**

So, the new list of deliverables for WP1 is

Deliverables

D1.1: PDK for sub 16 nm technology bulk MOSFETs including statistical variability and statistical reliability. (UOG) T0+12M

D1.2: PDK for sub 16 nm technology FinFET transistors including statistical variability and statistical reliability. (UOG) T0+18M

D1.3: PDK for sub 16 nm technology CNT including statistical variability and statistical reliability. (UPC) T0+27M

D1.4: PDK for sub 16 nm technology III-V/Ge CMOS transistors including statistical variability and statistical reliability. (UOG) T0+36M

While the original was:

Deliverables

D1.1: PDK for sub 16 nm technology bulk MOSFETs including statistical variability and statistical reliability. (UOG) T0+12M

D1.2: PDK for sub 16 nm technology CNT including statistical variability and statistical reliability. (UPC) T0+18M

D1.3: PDK for sub 16 nm technology FinFET transistors including statistical variability and statistical reliability. (UOG) T0+27M

D1.4: PDK for sub 16 nm technology III-V/Ge CMOS transistors including statistical variability and statistical reliability. (UOG) T0+36M

4. CHANGES IN WORK PACKAGE 2

No change of any deliverable order, date or description. The Only change is:

- **a reduction of the effort of IMEC in Task 2.3 of 4,5 pms, changing from 8,5 to 4 pms.**

This is more reasonable task effort considering that in this task 2.3 UPC has the strongest weight, and because of the need of increasing efforts of IMEC in the same quantity in WP4.

5. CHANGES IN WORK PACKAGE 3

- **D3.6 is related with the analysis of the sensitivity of cells to environmental and process variability. It was wrongly positioned as the last deliverable while it has to be the first.** In order to keep the same distribution, D3.6 changes from M36 to M12 and D3.1 moves from M12 to M24. The rest keeps the same.

The new list of deliverables is:

Deliverables

D3.1 Report on the effect of environmental and process parameters on the variability of the cell and system. (UPC) T0+M12.

D3.2 Report on mechanisms at layout and circuit level to mitigate variability. (UPC) T0+M24.

D3.3: Report on mechanisms to detect latency of SRAM cells accounting for operating conditions. (UPC) T0+M24.

D3.4 Report on new architectures for improving reliability based on redundancy. (UPC) T0+ M24.

D3.5: Report on the analysis of compensating and reconfiguration mechanisms for the memory cell and system to reduce the impact of variability and lack of reliability. (UPC) T0+M24.

D3.6: Report on the toolflow that instantiates the SKM knob insertion in SRAMs. (IMEC) T0+M36.

IMEC

While the original was:

Deliverables

D3.1 Report on mechanisms at layout and circuit level to mitigate variability. (UPC) T0+M12

D3.2 Report on new architectures for improving reliability based on redundancy. (UPC) T0+ M24

D3.3. Report on mechanisms to detect latency of SRAM cells accounting for operating conditions. (UPC) T0+M24

D3.4: Report on the analysis of compensating/reconfiguration mechanisms for the memory cell and system to reduce the impact of variability and lack of reliability. (UPC) T0+M24

D3.5: Report on the toolflow that instantiates the SKM knob insertion in SRAMs. (IMEC) T0+M36

D3.6: Report on the effect of environmental and process parameters on the variability of the cell. (UPC) T0+M36 and system.

6. CHANGES IN WORK PACKAGE 4

   - **The only change is the increase of 4.5 pms to IMEC (coming from WP2).** No other change.

7. WORK PACKAGES 5 and 6

   No change.